REMARKS

This paper responds to the Office Action mailed on October 27, 2003. Claims 50-52 are added. Claims 26-52 are pending in this application.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§102 Rejection of the Claims

Claims 26, 29, 32, 35-39 and 40 were rejected under 35 USC § 102(e) as being anticipated by Langendorf et al. (U.S. 6,505,282, "Langendorf"). Applicant respectfully traverses.

Applicant does not admit that Langendorf is prior art and reserves the right to swear behind Langendorf at a later date. Nonetheless, Applicant believes the present claims are distinguishable over Langendorf at least for the reasons stated below.

Langendorf apparently does not include all of the elements of the contested claims. Applicant is unable to find in Langendorf, among other things, a disclosure of burst extended data out mode as recited or incorporated into the claims. Burst extended data out mode (burst EDO) is defined in the present application to include, among other things, only one control line (CAS) toggling at the operating frequency as recited in claims 50 and 51, eliminating the need for external address lines to switch at high frequencies (*see* page 6 lines 5-13). In contrast, Langendorf refers to changing external address lines (*see* Langendorf, FIG. 6). Thus, Langendorf apparently does not include any disclosure of burst EDO mode.

Applicant respectfully requests reconsideration and allowance of claims 26, 29, 32, 35-39 and 40.

Claims 26, 29, 32, 35-39 and 40 were rejected under 35 USC § 102(a) as being anticipated "Intel" Electronic News, ("EN") December 5, 1994 in view of 82430FX PCIset DATASHEET 82537FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 ("INTEL"). Applicant respectfully traverses.

All elements are not disclosed

EN and INTEL apparently do not include all of the elements of the contested claims. Applicant is unable to find in EN and INTEL, among other things, a disclosure of burst EDO mode as recited or incorporated into the claims. Burst EDO mode is defined in the present application to include, among other things, eliminating the need for external address lines to switch at high frequencies (*see* page 6 lines 5-11). Instead, INTEL refers to the [memory array] lines being translated from the address lines for all memory accesses (see INTEL page 42, column 2). Also, the performance of the memory accesses in INTEL are measured with respect to a time from Address Status asserted to Bus Ready asserted (see INTEL page 45, Table 11). Further, the EN reference is silent as to memory modes. Thus, EN and INTEL apparently do not include any disclosure of burst EDO mode as defined in the present claims.

Regarding the two reference 102(a) rejection:

The rejection uses two references in rejecting the contested claims under 35 U.S.C. § 102(a).

As discussed above, the two references in combination do not show all of the elements in the contested claims.

Also, under 35 U.S.C. § 102(a), an Applicant is denied a patent when the invention was used or known by another, or was patented or described in a printed publication before the invention by the Applicant. If the EN reference is being used as a rejection due to a printed publication, the references do not qualify for the rejection. The EN reference from December 5, 1994 merely states that "Intel is readying the Triton PCI chipset, which it was demonstrating privately during Fall Comdex," and does not describe any principle of operation of the memory modes. Memory modes are described in the INTEL reference which is dated November 1996, and the EN reference cannot be used to predate the INTEL reference. Thus, because the cited printed publication that describes memory modes is dated November 1996, the references do not qualify as printed publications under § 102(a) since the present application claims priority under

CIP status at least as far back as December 23, 1994. Thus, in the alternative, Applicant assumes the EN reference is being used in the Office Action to show that the invention was used or known by another.

If so, the EN reference is too vague to prove an invention was used or known by another. The EN reference states that the PCI chipset is being readied, and does not elaborate on what is meant by "demonstrated privately," possibly implying the PCI chipset was not reduced to practice at Comdex. The INTEL reference does not resolve this vagueness. INTEL can only provide extrinsic evidence as of the date of its publication -- November 1996.

The MPEP states a standard necessary for multiple references to show that a characteristic not disclosed in the reference is inherent. It states, "to serve as anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by person of ordinary skill" (MPEP 2143.01).

Applicant submits that the references fail to meet the standard. INTEL only provides extrinsic evidence pertaining to memory modes as of November 1996 (its date of publication) and does not show what was necessarily present in EN on December 5, 1994. And further, Applicant submits that what was present as of November 1996 does not show all of the elements in the contested claims.

Reliance on MPEP 2124 and 2131.01 is incorrect

In order for the examiner to use INTEL it must fall under one of the narrow exceptions to the rule that a non-patent document must predate the filing date of the application. Some narrow instances where a document need not antedate the filing date are set forth in MPEP §2124. The examiner cites MPEP §2124 for supporting his use of INTEL as prior art in rejecting the claims under 35 U.S.C. §102(a). MPEP 2124 provides exception to the rule that the critical reference date must precede the filing date of an application. MPEP 2124 states

> In certain circumstances, references cited to show a universal fact need not be available as prior art before applicant's filing date. In re Wilson, 311 F.2d 266, 135 USPQ 442 (CCPA 1962). Such facts include the characteristics and properties of a material or a scientific truism. Some specific examples in which later publications showing factual evidence can be cited include

> situations where the facts shown in the reference are evidence "that, as of an application's filing date, undue experimentation would have been required, In re Corneil, 347 F.2d 563, 568, 145 USPQ 702, 705 (CCPA 1965), or that a parameter absent from the claims was or was not critical, In re Rainer, 305 F.2d 505, 507 n.3, 134 USPQ 343, 345 n.3 (CCPA 1962), or that a statement in the specification was inaccurate, In re Marzocchi, 439 F.2d 220, 223 n.4, 169 USPQ 367, 370 n.4 (CCPA 1971), or that the invention was inoperative or lacked utility, In re Langer, 503 F.2d 1380, 1391, 183 USPQ 288, 297 (CCPA 1974), or that a claim was indefinite, In re Glass, 492 F.2d 1228,1232 n.6, 181 USPQ 31, 34 n.6 (CCPA 1974), or that characteristics of prior art products were known, In re Wilson, 311 F.2d 266, 135 USPQ 442 (CCPA 1962)." In re Koller, 613 F.2d 819, 823 n.5, 204 USPQ 702, 706 n.5 (CCPA 1980) (quoting In re Hogan, 559 F.2d 595, 605 n.17, 194 USPQ 527, 537 n.17 (CCPA 1977) (emphasis in original)). However, it is impermissible to use a later factual reference to determine whether the application is enabled or described as required under 35 U.S.C. 112, first paragraph. In re Koller, 613 F.2d 819, 823 n. 5, 204 USPQ 702, 706 n.5 (CCPA 1980). References which do not qualify as prior art because they postdate the claimed invention may be relied upon to show the level of ordinary skill in the art at or around the time the invention was made. Ex parte Erlich, 22 USPQ 1463 (Bd. Pat. App. & Inter. 1992).

Applicant requests that the examiner indicate the specific basis for reliance on this MPEP section to clarify issues for appeal. Applicant submits that INTEL does not prove the characteristics and properties of a material or a scientific truism.

Based on the undersigned's reading of MPEP 2124, the examiner appears to be relying on In re Wilson. Applicant respectfully submits that such reliance is misplaced. Wilson allows the use of publications that have a date after the filing date of the application to prove a universal fact. The court in Wilson first found the claims at issue to be obvious in view of acknowledged prior art and a prior art reference. The admitted prior art and the prior art reference both predated the application filing date. Thus, two pieces of prior art as defined by the statute were applied in a §103 rejection. The court did not use the publication that is subsequent to the application filing date to prove a case of *prima facie* anticipation under §102(a).

The appellant-applicant in Wilson further asserted a factual advantageous feature that resulted from the claimed inventive chemical process. The court then used the publication to

create a factual suspicion on the appellant-applicant's assertion of a factual advantageous feature from the claimed chemical process.[1]

Based on Wilson, the examiner's reliance on EN to read INTEL as prior art is misplaced. First, a *prima facie* case of obviousness has not been established based on prior art that one of ordinary skill had at the time of the present invention. That is, the examiner can not rely on INTEL in a rejection under §102(a).

Accordingly, because all of the elements recited in the claims are not found in EN and INTEL and because reliance on EN to read INTEL as prior art is misplaced, applicant respectfully requests that the §102(a) rejection of the pending claims 26, 29, 32, 35-39 and 40 based in part on EN and INTEL be withdrawn and that the claims be reconsidered and allowed.

§103 Rejection of the Claims

Claims 27-28, 30-31, 33, 34, and 41-49 were rejected under 35 USC § 103(a) as being anticipated by Langendorf et al. in view of Suzuki et al. (U.S. 5,787,308, "Suzuki"). Applicant respectfully traverses.

To establish proper *prima facie* obviousness all claim limitations must be taught or suggested by the prior art.

Applicant is unable to find in the cited portions of the proposed combination of Langendorf and Suzuki, among other things, any disclosure of burst EDO mode as recited or incorporated into the claims. As discussed previously, Langendorf refers to changing external address lines (*see* Langendorf, FIG. 6) and apparently does not include any disclosure of burst EDO mode. Also, Applicant cannot find any discussion of memory modes in the cited portions of Suzuki.

Also, the proposed combination of references must provide the motivation (teaching, suggestion, or incentive) to modify the references. Because Langenford refers to detection logic to program a memory controller and because the cited portions of Suzuki refer to I/O initialization and are apparently silent as to memory initialization, Applicant submits that such motivation is lacking.

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[1] In re Wilson and Lieberman, 135 USPQ 442, 446 (CCPA 1962).

Because the proposed combination fails to teach or suggest all of the elements of the contested claims and because motivation to make the proposed combination is apparently lacking, Applicant respectfully requests reconsideration and allowance of claims 27-28, 30-31, 33, 34, and 41-49.

Claims 27-28, 30-31, 33, 34, and 41-49 were rejected under 35 USC § 103(a) as being anticipated by "Intel" Electronic News, ("EN") December 5, 1994 in view of 82430FX PCIset DATASHEET 82537FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 ("INTEL") and further in view of Suzuki et al. Applicant respectfully traverses.

Generally, a non-patent document is prior art and can be used in rejecting claims under 35 U.S.C. §103 if its publication date precedes the filing date of the application. The present application is a continuation of an application that was filed on June 1, 1995, which claims CIP status to an application filed December 23, 1994. The INTEL document has a publication date of November 1996. Clearly, well over a year -- at least about 15 months -- after the effective filing date of the present application. Accordingly, INTEL is not available as a prior art document under the basic rule for available prior art for use in 35 U.S.C. §103 rejections.

Also, as discussed previously in regards to the rejection under 35 U.S.C. § 102(a), EN and INTEL apparently do not include all of the elements of the contested claims. Applicant is unable to find in EN and INTEL, among other things, a disclosure of burst EDO mode as recited or incorporated into the claims. The addition of Suzuki does not provide the missing elements at least for the reason that Suzuki is also silent as to burst EDO mode.

Also, the Office Action refers to a processor programming a memory controller in Suzuki. However, Applicant is unable to find such disclosure in the cited portions of Suzuki.

Because the proposed combination fails to teach or suggest all of the elements of the contested claims, and because INTEL is not available as a prior art document, Applicant respectfully requests reconsideration and allowance of claims 27-28, 30-31, 33, 34, and 41-49.

Claims 26, 29, 32, and 35-39 were rejected under 35 USC § 103(a) as being anticipated by Farrer et al. (U.S. 5,307,320, "Farrer") in view of Micron, "Reduce DRAM cycle times with

extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 ("MICRON") and further in view of Wyland (U.S. 5,261,064). Applicant respectfully traverses.

Applicant submits that there is no motivation in the prior art to make the proposed combination. Wyland refers to interleaving in achieving its burst mode (*see* column 3 lines 43-46). MICRON refers to page interleaving causing bus contention in EDO mode (*see* page 5-39, column 2). Thus, because of this conflict as to the advantages of interleaving, motivation is apparently lacking to make a combination of MICRON with Wyland.

Also, the proposed combination of references fails to establish *prima facie* obviousness because the combination does not provide an incentive to modify the references to provide the claimed invention. The mere fact that the prior art could be modified to provide the claimed invention is not sufficient to establish obviousness, there must be motivation (i.e. a teaching, suggestion, or incentive) in the prior art to make the modification. Applicant is unable to find any teaching or suggestion or incentive in the proposed combination for providing burst EDO mode.

Further, the prior art must be considered in its entirety, including disclosures that teach away from the invention. The present application teaches that an advantage of burst EDO is that interleaving is not required (*see* page 7, lines 1-3). Applicant submits that, at least for the reason that Wyland refers to interleaving, a combination including Wyland teaches away from the burst operation of the present invention.

Furthermore, Applicant cannot find in the cited portions of the proposed combination of Farrer, MICRON and Wyland, among other things, any disclosure of, wherein the processor is responsive to at least information from the memory to program the memory controller ... , wherein the information from the memory includes data read from the memory device, as recited or incorporated into the claims.

Therefore, because motivation is lacking to make the proposed combination, because the proposed combination teaches away from the claimed invention, and because all elements of the claims are not taught or suggested in the proposed combination of references, Applicant respectfully requests reconsideration and allowance of claims 26, 29, 32, and 35-39.

Claims 27-28, 30-31, 33, 34 and 41-49 were rejected under 35 USC § 103(a) as being anticipated by Farrer et al. in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and Wyland and further in view of Suzuki et al. Applicant respectfully traverses.

Applicant repeats the discussion of the problems with the proposed combination of Farrer, MICRON and Wyland. The proposed addition of Suzuki does not resolve the aforementioned problems.

Also, Applicant is unable to find a teaching or suggestion of,

> a ... power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller; wherein the processor is responsive to at least information from the memory to program the memory controller ..., wherein the information from the memory includes data read from the memory device,

as recited or incorporated in the claims.

Therefore, because of the aforementioned problems with a combination of Farrer, MICRON and Wyland, and because all elements of the claims are not taught or suggested in the proposed combination of references, Applicant respectfully requests reconsideration and allowance of claims 27-28, 30-31, 33, 34 and 41-49.

Applicant incorporates all prior responses by reference to preserve all issues for appeal.

New Claims

Claims 50-52 are new. Support for the new claims is found generally within the specification (*see* e.g., page 6, lines 5-13, and page 15, lines 4-12). Applicant requests entry and examination of the new claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 27th day of February, 2004.

Amy Moriarty
Name

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Signature